



CSD23381F4, 12 V P-Channel FemtoFET™ MOSFET

1 Features

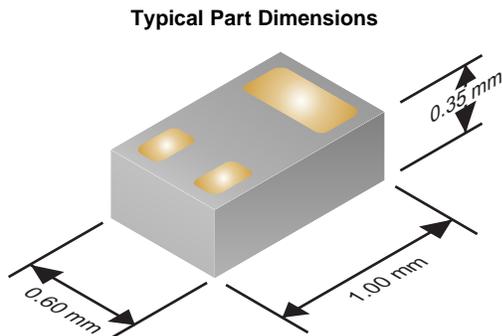
- Ultra-Low On Resistance
- Ultra-Low Q_g and Q_{gd}
- High Operating Drain Current
- Ultra-Small Footprint (0402 Case Size)
 - 1.0 mm x 0.6 mm
- Ultra-Low Profile
 - 0.35 mm Max Height
- Integrated ESD Protection Diode
 - Rated > 4 kV HBM
 - Rated > 2 kV CDM
- Lead and Halogen Free
- RoHS Compliant

2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Battery Applications
- Handheld and Mobile Applications

3 Description

This 150 m Ω , 12 V P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.



Product Summary

V_{DS}	Drain-to-Source Voltage	-12	V
Q_g	Gate Charge Total (-4.5 V)	1140	pC
Q_{gd}	Gate Charge Gate to Drain	190	pC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = -1.8$ V	480 m Ω
		$V_{GS} = -2.5$ V	250 m Ω
		$V_{GS} = -4.5$ V	150 m Ω
$V_{GS(th)}$	Threshold Voltage	-0.95	V

Ordering Information

Device	Qty	Media	Package	Ship
CSD23381F4	3000	7-Inch Reel	Femto(0402) 1.0 mm x 0.6 mm Land Grid Array (LGA)	Tape and Reel
CSD23381F4T	250			

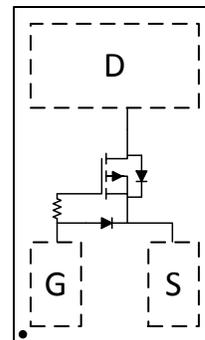
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	-12	V
V_{GS}	Gate-to-Source Voltage	-8	V
I_D	Continuous Drain Current ⁽¹⁾	-2.3	A
I_{DM}	Pulsed Drain Current ⁽²⁾	-9	A
I_G	Continuous Gate Clamp Current	-35	mA
	Pulsed Gate Clamp Current ⁽²⁾	-350	
P_D	Power Dissipation ⁽¹⁾	500	mW
ESD Rating	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	2	kV
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

(1) Typical $R_{\theta JA} = 85^\circ\text{C/W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤ 300 μs , duty cycle $\leq 2\%$

Top View



4 Specifications

4.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_{DS} = -250\ \mu\text{A}$	-12			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$			-100	nA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = -12\text{ V}$			-50	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = -250\ \mu\text{A}$	-0.70	-0.95	-1.20	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = -1.8\text{ V}, I_{DS} = -0.1\text{ A}$		480	970	m Ω
		$V_{GS} = -2.5\text{ V}, I_{DS} = -0.5\text{ A}$		250	300	m Ω
		$V_{GS} = -4.5\text{ V}, I_{DS} = -0.5\text{ A}$		150	175	m Ω
g_{fs}	Transconductance	$V_{DS} = -6\text{ V}, I_{DS} = -0.5\text{ A}$		2.0		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = -6\text{ V},$ $f = 1\text{ MHz}$		236		pF
C_{oss}	Output Capacitance			98		pF
C_{rss}	Reverse Transfer Capacitance			6.9		pF
R_G	Series Gate Resistance			20		Ω
Q_g	Gate Charge Total (4.5 V)	$V_{DS} = -6\text{ V}, I_{DS} = -0.5\text{ A}$		1140		pC
Q_{gd}	Gate Charge Gate to Drain			190		pC
Q_{gs}	Gate Charge Gate to Source			300		pC
$Q_{g(th)}$	Gate Charge at V_{th}			145		pC
Q_{oss}	Output Charge		$V_{DS} = -6\text{ V}, V_{GS} = 0\text{ V}$		1290	
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 0\text{ V}, V_{GS} = -4.5\text{ V},$ $I_{DS} = -0.5\text{ A}, R_G = 2\ \Omega$		4.5		ns
t_r	Rise Time			3.9		ns
$t_{d(off)}$	Turn Off Delay Time			18.0		ns
t_f	Fall Time			7.0		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{SD} = -0.5\text{ A}, V_{GS} = 0\text{ V}$		-0.75		V
Q_{rr}	Reverse Recovery Charge	$V_{DS} = -10\text{ V}, I_F = -0.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		1260		pC
t_{rr}	Reverse Recovery Time			7.9		ns

4.2 Thermal Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

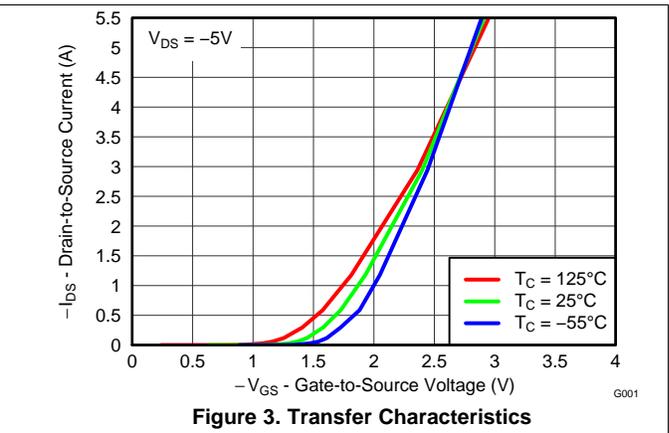
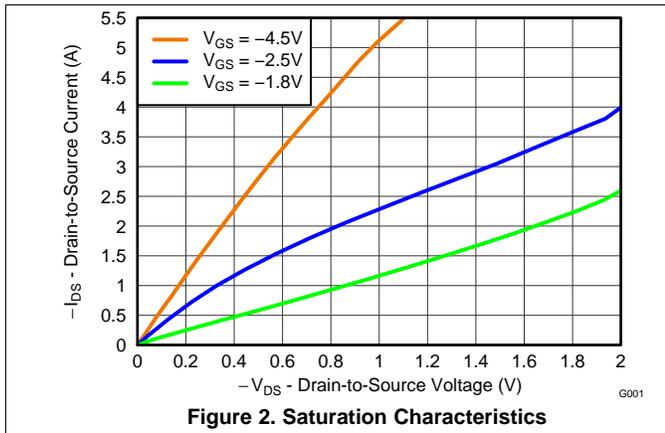
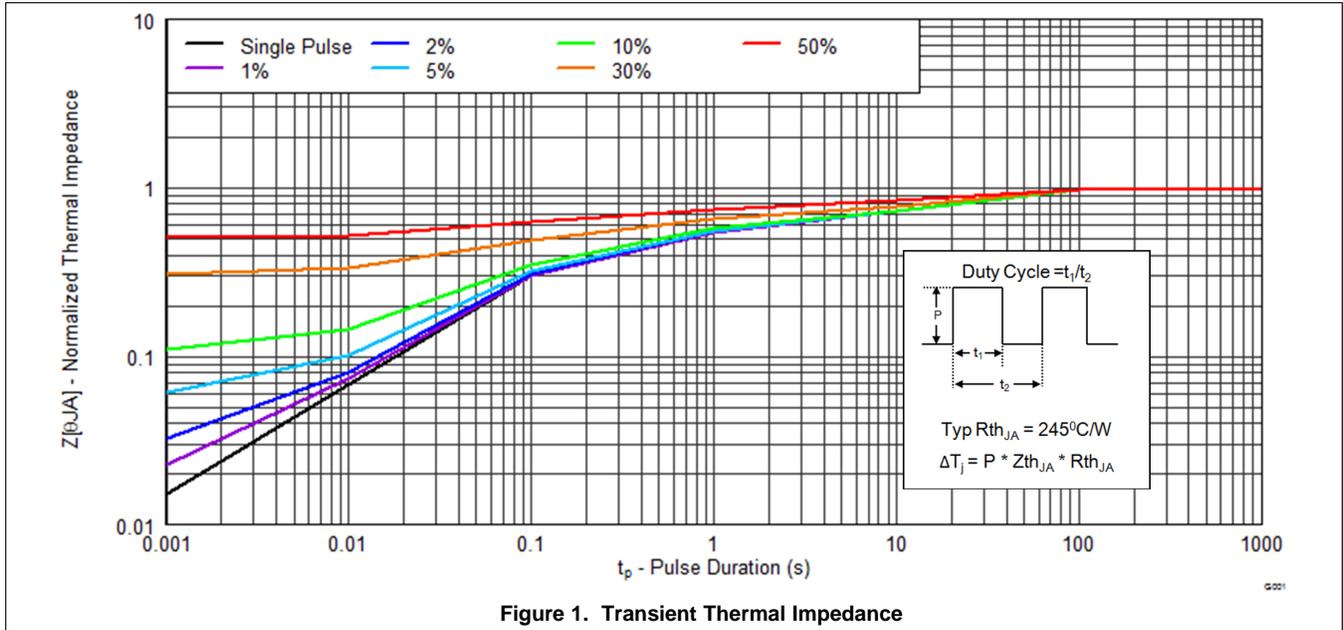
PARAMETER		Typical Values	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾	85	$^\circ\text{C}/\text{W}$
	Junction-to-Ambient Thermal Resistance ⁽²⁾	245	$^\circ\text{C}/\text{W}$

(1) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

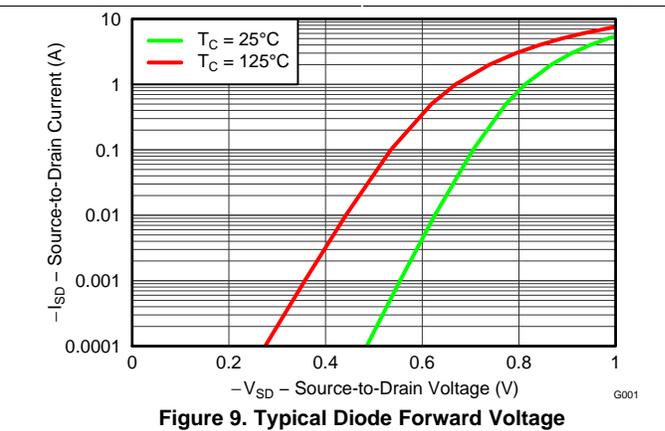
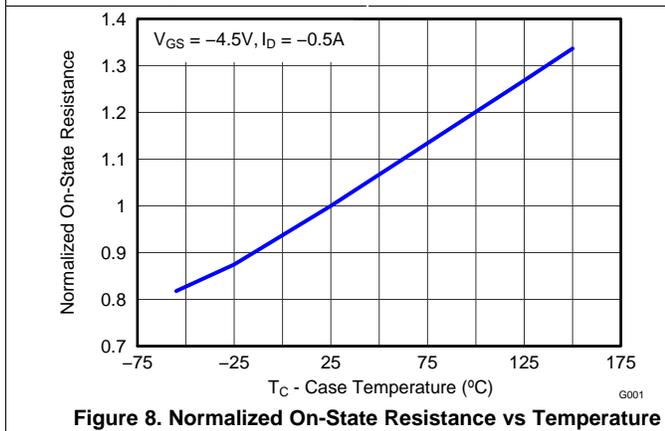
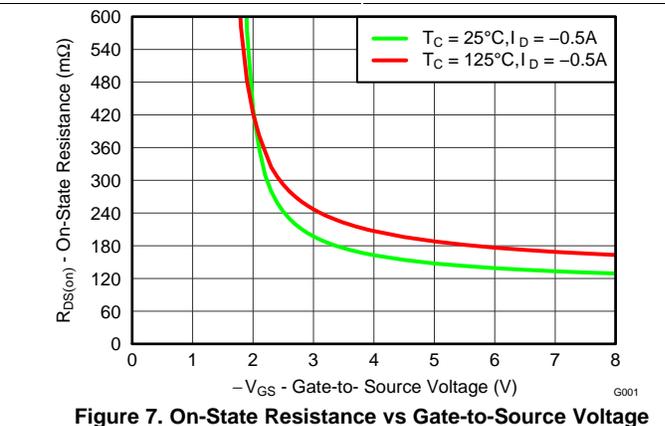
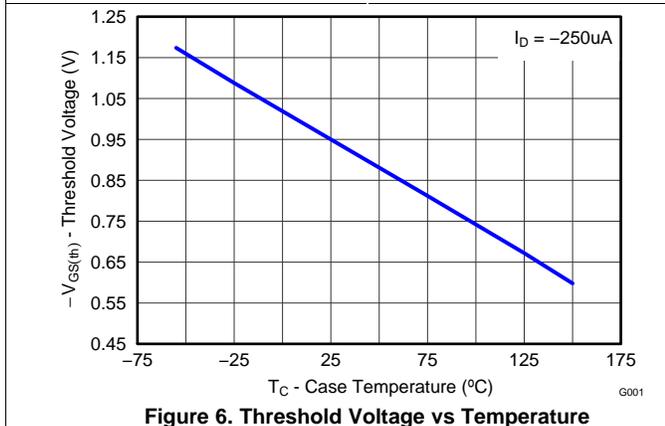
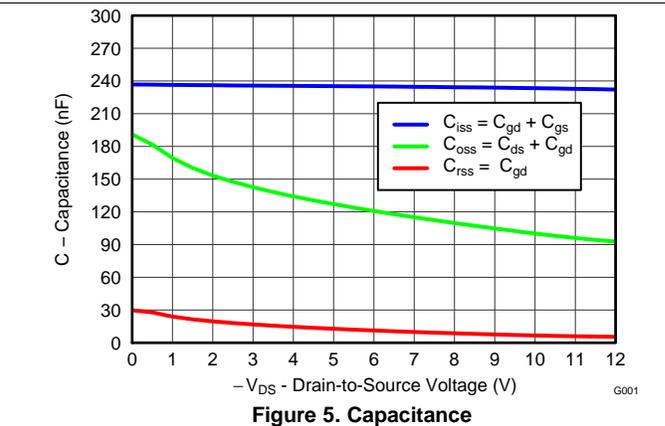
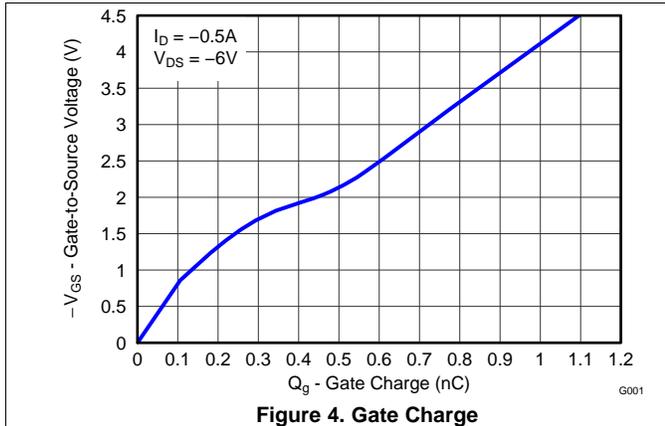
5 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

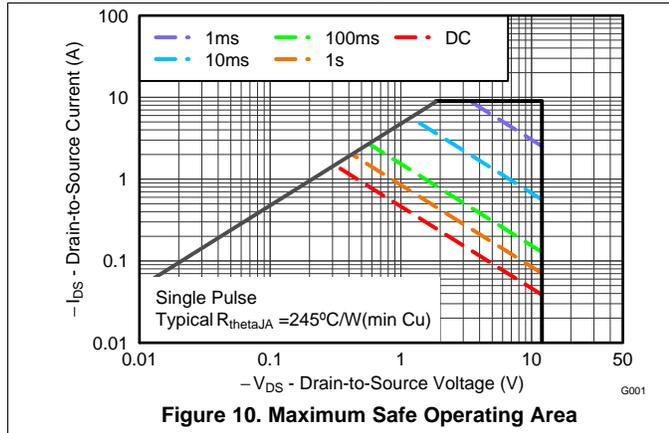


Figure 10. Maximum Safe Operating Area

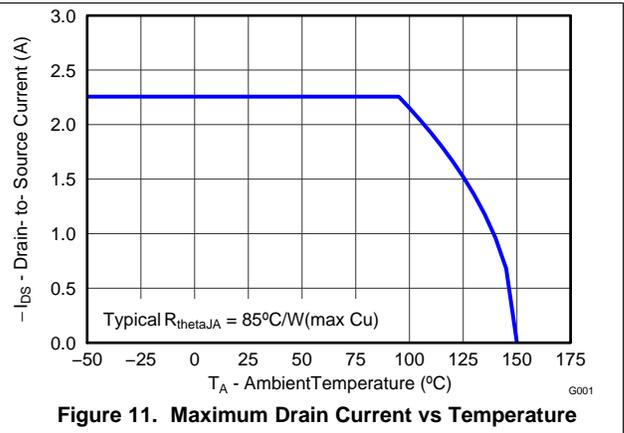
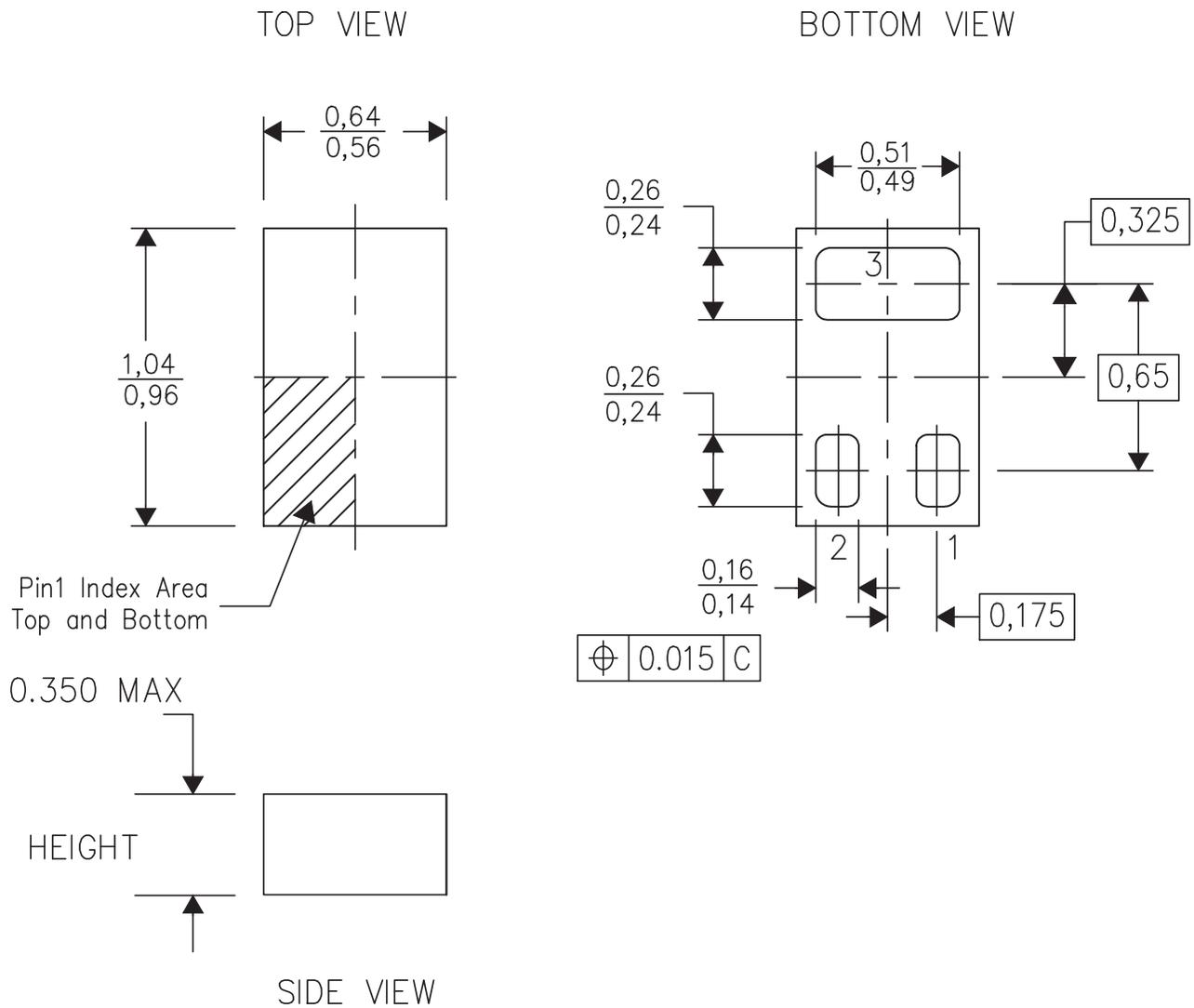


Figure 11. Maximum Drain Current vs Temperature

6 Mechanical Data

6.1 0402 Mechanical Dimensions

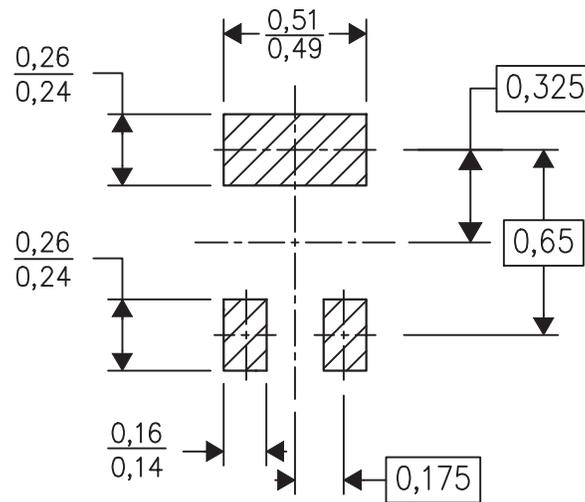


- (1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- (2) This drawing is subject to change without notice.
- (3) This package is a PB-free solder land design.

Pin Configuration

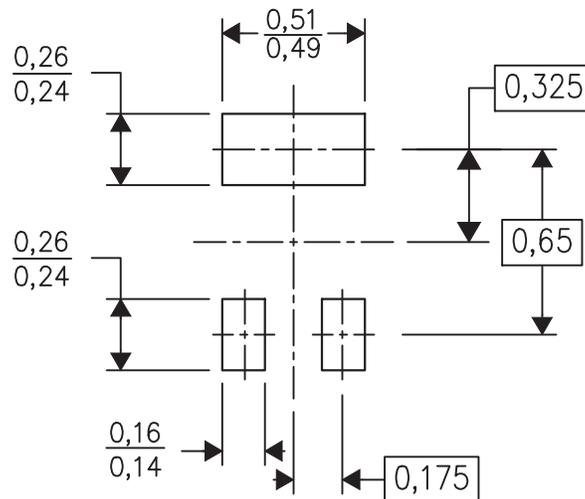
Position	Designation
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

6.2 Recommended Minimum PCB Layout



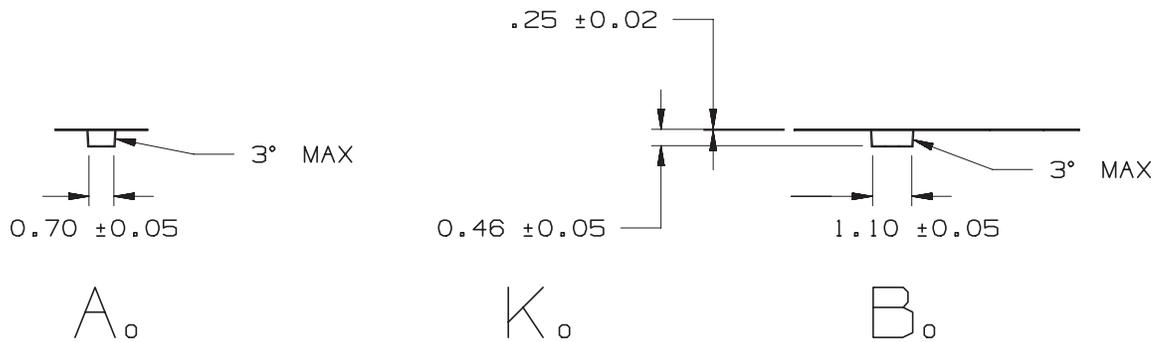
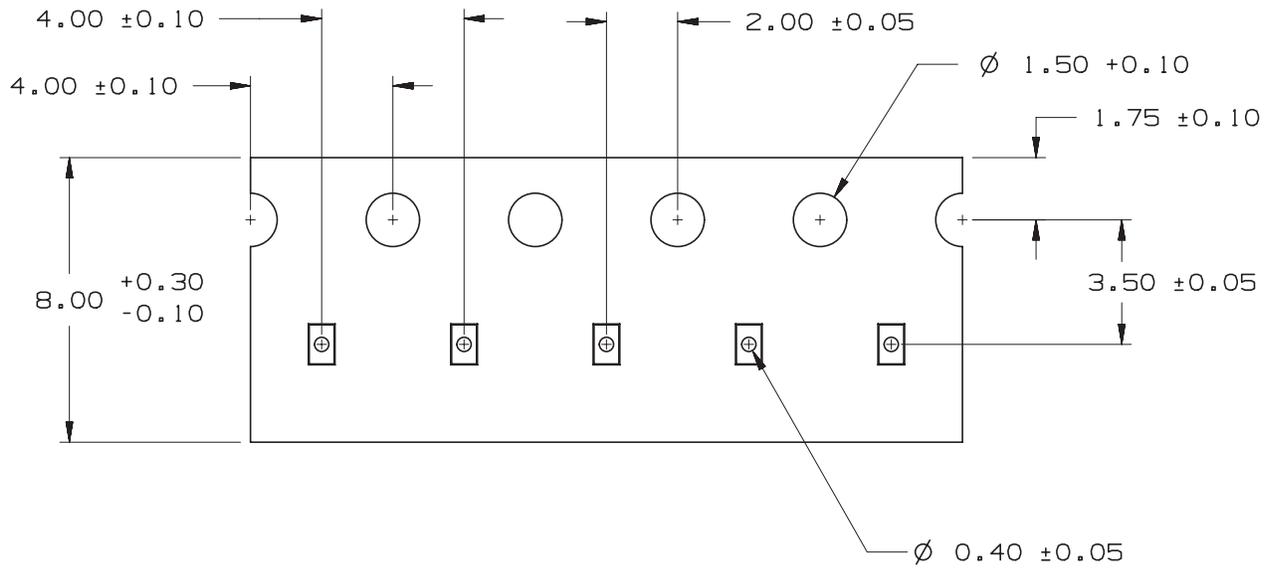
(1) All dimensions are in millimeters.

6.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

6.4 CSD23381F4 Embossed Carrier Tape Dimensions



- (1) Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

7 Trademarks

FemtoFET is a trademark of Texas Instruments.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2014) to Revision B	Page
• Updated lead and halogen free in features	1
• Added I_G parameter	1
• Lowered I_{DSS} limit	2
• Lowered I_{GSS} limit	2

Changes from Original (October 2013) to Revision A	Page
• Updated title	1
• Added small reel info	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23381F4	ACTIVE	PICOSTAR	YJC	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-250C-UNLIM	-40 to 85	DS	Samples
CSD23381F4R	PREVIEW	PICOSTAR	YJC	3	18000	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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